

In the Claims

Please amend the claims as follows:

1 1. (Currently Amended) A method of data transfer between a  
2 source port and a destination port of a transfer controller with  
3 plural ports, said method comprising the steps of:

4 in response to a data transfer request, querying said  
5 destination port to determine if said destination port is capable  
6 of receiving data of a predetermined size;

7 if said destination port is not capable of receiving data of  
8 said predetermined size, waiting by not reading data of said  
9 predetermined size from said source port corresponding to said data  
10 transfer request and not transferring data to said destination port  
11 until said destination port is capable of receiving data, and

12 if said destination port is capable of receiving data of said  
13 predetermined size, reading data of said predetermined size from  
14 said source port and transferring said read data to said  
15 destination port.

1 2. (Currently Amended) The method of claim 1, wherein each  
2 port includes at least one write reservation station, said method  
3 wherein:

4 said step of querying said destination port includes:

5 determining whether any write reservation station of said  
6 destination port has not been allocated for receipt of data,  
7 and

8 if at least one write reservation is not allocated for  
9 receipt of data, determining said destination port can receive  
10 data and allocating a write reservation station for receipt of  
11 data; and

12 said step of transferring said read data to said destination  
13 port includes transferring said read data to said allocated write  
14 reservation station of said destination port.

95 1 3. (Original) The method of claim 2, further comprising:  
2 transferring data from a write reservation station storing  
3 data to be transferred to an application unit coupled to said  
4 destination port at a data transfer rate of said application unit;  
5 and  
6 disallocating said write reservation station upon transfer of  
7 data to said application unit.

1 4. (Original) The method of claim 2, wherein:  
2 said step of allocating a write reservation station includes  
3 storing a data identifier corresponding to said write reservation  
4 station; and  
5 said step of transferring said read data to said destination  
6 port includes storing said read data in a write reservation station  
7 having a data identifier corresponding to said read data.

1 5. (Currently Amended) The method of claim 1, further  
2 comprising:  
3 while waiting until said destination port is capable of  
4 receiving data  
5 determining if a second data transfer request is pending  
6 between said source port and a second destination port, and  
7 if a second data transfer request is pending, ~~servicing~~  
8 ~~said second data transfer~~  
9 querying said second destination port to determine  
10 if said second destination port is capable of receiving  
11 data of said predetermined size,

12 if said second destination port is not capable of  
13 receiving data of said predetermined size, waiting by not  
14 reading data of said predetermined size from said source  
15 port corresponding to said second data transfer request  
16 until said second destination port is capable of  
17 receiving data, and

18 if said second destination port is capable of  
19 receiving data of said predetermined size, reading data  
20 of said predetermined size from said source port and  
21 transferring said read data to said second destination  
22 port.

✓ 6. (Canceled)

1 7. (Currently Amended) A data transfer controller comprising:  
2 a request queue controller receiving, prioritizing and  
3 dispatching data transfer requests, each data transfer request  
4 specifying a data source, a data destination and a data quantity to  
5 be transferred;

6 a data transfer hub connected to request queue controller  
7 effecting dispatched data transfer requests;

8 a plurality of ports, each of said plurality of ports having  
9 an interior interface connected to said data transfer hub and an  
10 exterior interface configured for an external memory/device  
11 expected to be connected to said port, said interior interface and  
12 said exterior interface operatively connected for data transfer  
13 therebetween; and

14 said data transfer hub controlling data transfer from a source  
15 port corresponding to said data source to a destination port  
16 corresponding to said data destination in a quantity corresponding  
17 to said data quantity to be transferred of a currently executing

18 data transfer request, said data transfer hub further controlling  
19 said source port and said destination port to

20 in response to a data transfer request, query said  
21 destination port to determine if said destination port is  
22 capable of receiving data of a predetermined size,

23 if said destination port is not capable of receiving data  
24 of said predetermined size, waiting by not reading data of  
25 said predetermined size from said source port corresponding to  
26 said data transfer request and not transferring data to said  
27 destination port until said destination port is capable of  
28 receiving data, and

29 if said destination port is capable of receiving data of  
30 said predetermined size, reading data of said predetermined  
31 size from said source port and transferring said read data to  
32 said destination port.

1 8. (Currently Amended) The data transfer controller of claim  
2 7, wherein:

3 each port includes at least one write reservation station for  
4 storing data prior to transfer to said corresponding external  
5 memory/device;

6 said data transfer hub further controlling said destination  
7 port to

8 determine whether any write reservation station of said  
9 destination port has not been allocated for receipt of data,  
10 and

11 if at least one write reservation is not allocated for  
12 receipt of data, determining said destination port can receive  
13 data and allocating a write reservation station for receipt of  
14 data, and

15 transfer said read data to said allocated write  
16 reservation station of said destination port.

1 9. (Original) The data transfer controller of claim 8,  
2 wherein:

3 said data transfer hub further controlling said destination  
4 port to

5 transfer data from a write reservation station to said  
6 corresponding external memory/device at a data transfer rate  
7 of said external memory/device, and

8 disallocating said write reservation station upon  
9 transfer of data from said write reservation station to said  
10 external memory/device.

1 10. (Currently Amended) The data transfer controller of claim  
2 8, wherein:

3 each of said plurality of ~~hubs~~ ports further includes an  
4 identifier register corresponding to each write reservation  
5 station; and

6 said data transfer hub further controlling said destination  
7 port to

8 allocate a write reservation station by writing  
9 identifier data in said corresponding identifier register, and

10 store said read data in a write reservation station  
11 having a corresponding identifier stored in said identifier  
12 register corresponding to said write reservation station.

1 11. (Currently Amended) The data transfer controller of claim  
2 ~~±~~ 7, wherein:

3 said data transfer ~~controller~~ hub further capable of ~~servicing~~  
4 ~~a second transfer request between said source port and a second~~  
5 ~~destination port~~ while waiting until said destination port is  
6 capable of receiving data of

7        determining if a second data transfer request between  
8        said source port and a second destination port is pending,  
9        if a second data transfer request is pending  
10        querying said second destination port to determine  
11        if said second destination port is capable of receiving  
12        data of said predetermined size,  
13        if said second destination port is not capable of  
14        receiving data, waiting by not reading data of said  
15        predetermined size from said source port corresponding to  
16        said second data transfer request until said second  
17        destination port is capable of receiving data, and  
18        if said second destination port is capable of  
19        receiving data, reading data of said predetermined size  
20        from said source port and transferring said read data to  
21        said second destination port.

12. (Canceled)

1        13. (Currently Amended) A data processing system comprising:  
2        a plurality of data processors, each data processor capable of  
3        generating a data transfer request;  
4        a request queue controller connected to said plurality of data  
5        processors, said request queue controller receiving, prioritizing  
6        and dispatching data transfer requests, each data transfer request  
7        specifying a data source, a data destination and a data quantity to  
8        be transferred;  
9        a data transfer hub connected to request queue controller  
10        effecting dispatched data transfer requests;  
11        a plurality of ports, each of said plurality of ports having  
12        an interior interface connected to said data transfer hub  
13        identically configured for each port and an exterior interface  
14        configured for an external memory/device expected to be connected

15 to said port, said interior interface and said exterior interface  
16 operatively connected for data transfer therebetween; and

17 said data transfer hub controlling data transfer from a source  
18 port corresponding to said data source to a destination port  
19 corresponding to said data destination in a quantity corresponding  
20 to said data quantity to be transferred of a currently executing  
21 data transfer request, said data transfer hub further controlling  
22 said source port and said destination port to

23 in response to a data transfer request, query said  
24 destination port to determine if said destination port is  
25 capable of receiving data of a predetermined size,

26 if said destination port is not capable of receiving data  
27 of said predetermined size, waiting by not reading data of  
28 said predetermined size from said source port corresponding to  
29 said data transfer request and not transferring data to said  
30 destination port until said destination port is capable of  
31 receiving data, and

32 if said destination port is capable of receiving data of  
33 said predetermined size, reading data of said predetermined  
34 size from said source port and transferring said read data to  
35 said destination port.

1 14. (Currently Amended) The data processing system of claim  
2 13, wherein:

3 each port includes at least one write reservation station for  
4 storing data prior to transfer to said corresponding external  
5 memory/device;

6 said data transfer hub further controlling said destination  
7 port to

8 determine whether any write reservation station of said  
9 destination port has not been allocated for receipt of data,  
10 and

11 if at least one write reservation is not allocated for  
12 receipt of data, determining said destination port can receive  
13 data and allocating a write reservation station for receipt of  
14 data, and  
15 transfer said read data to said allocated write  
16 reservation station of said destination port.

AS 1 15. (Original) The data processing system of claim 14,  
2 wherein:

3 said data transfer hub further controlling said destination  
4 port to

5 transfer data from a write reservation station to said  
6 corresponding external memory/device at a data transfer rate  
7 of said external memory/device, and

8 disallocate said write reservation station upon transfer  
9 of data from said write reservation station to said external  
10 memory/device.

1 16. (Original) The data processing system of claim 14,  
2 wherein:

3 each of said plurality of hubs further includes an identifier  
4 register corresponding to each write reservation station; and

5 said data transfer hub further controlling said destination  
6 port to

7 allocate a write reservation station by writing  
8 identifier data in said corresponding identifier register, and

9 store said read data in a write reservation station  
10 having a corresponding identifier stored in said identifier  
11 register corresponding to said write reservation station.

1 17. (Currently Amended) The data processing system of claim  
2 13, wherein:



3 said data transfer ~~controller~~ hub further capable of ~~servicing~~  
4 ~~a second transfer request between said source port and a second~~  
5 ~~destination port~~ while waiting until said destination port is  
6 capable of receiving data of

7 determining if a second data transfer request between  
8 said source port and a second destination port is pending,  
9 if a second data transfer request is pending

10 querying said second destination port to determine  
11 if said second destination port is capable of receiving  
12 data of said predetermined size,

13 if said second destination port is not capable of  
14 receiving data, waiting by not reading data of said  
15 predetermined size from said source port corresponding to  
16 said second data transfer request until said second  
17 destination port is capable of receiving data, and

18 if said second destination port is capable of  
19 receiving data, reading data of said predetermined size  
20 from said source port and transferring said read data to  
21 said second destination port.

✓ 18. (Canceled)

1 19. (Currently Amended) The data processing system of claim  
2 13, further comprising:

3 said plurality of ports includes an internal port master;  
4 a data transfer bus connected to said internal port master and  
5 each of said data processors, said data transfer bus transferring  
6 data between said plurality of data processors and said data  
7 transfer hub via said internal port master;

8 a system memory connected to a predetermined one of said  
9 plurality of ports; and

10 wherein each of said data processors includes an instruction  
11 cache connected to said data transfer bus for temporarily storing  
12 program instructions controlling said data processor, said data  
13 processor generating a data transfer request to said request queue  
14 controller for ~~program~~ instruction cache fill from said system  
15 memory to said instruction cache upon a read access miss to said  
16 instruction cache.

AS 1 20. (Currently Amended) The data processing system of claim  
2 13, further comprising:

3 said plurality of ports includes an internal port master;  
4 a data transfer bus connected to said internal port master and  
5 each of said data processors, said data transfer bus transferring  
6 data between said plurality of data processors and said data  
7 transfer hub via said internal port master;

8 a system memory connected to a predetermined one of said  
9 plurality of ports; and

10 wherein each of said data processors includes a data cache  
11 connected to said data transfer bus for temporarily storing data  
12 employed by said data processor, said data processor generating a  
13 data transfer request to said request queue controller for data  
14 cache fill from said system memory to said data cache upon a read  
15 access miss to said data cache.

1 21. (Currently Amended) The data processing system of claim  
2 13, further comprising:

3 said plurality of ports includes an internal port master;  
4 a data transfer bus connected to said internal port master and  
5 each of said data processors, said data transfer bus transferring  
6 data between said plurality of data processors and said data  
7 transfer hub via said internal port master;

8 a system memory connected to a predetermined one of said  
9 plurality of ports; and

10 wherein each of said data processors includes a data cache  
11 connected to said data transfer bus for temporarily storing data  
12 employed by said data processor, said data processor generating a  
13 data transfer request to said request queue controller for data  
14 writeback from said data cache to said system memory upon a write  
15 miss to said data cache.

1 22. (Currently Amended) The data processing system of claim  
2 13, further comprising:

3 said plurality of ports includes an internal port master;  
4 a data transfer bus connected to said internal port master and  
5 each of said data processors, said data transfer bus transferring  
6 data between said plurality of data processors and said data  
7 transfer hub via said internal port master;

8 a system memory connected to a predetermined one of said  
9 plurality of ports; and

10 wherein each of said data processors includes a data cache  
11 connected to said data transfer bus for temporarily storing data  
12 employed by said data processor, said data processor generating a  
13 data transfer request to said request queue controller for write  
14 data allocation from said system memory to said data cache upon a  
15 write miss to said data cache.

1 23. (Currently Amended) The data processing system of claim  
2 13, further comprising:

3 said plurality of ports includes an internal port master;  
4 a data transfer bus connected to said internal port master and  
5 each of said data processors, said data transfer bus transferring  
6 data between said plurality of data processors and said data  
7 transfer hub via said internal port master;

8 a system memory connected to a predetermined one of said  
9 plurality of ports; and

10 wherein each of said data processors includes a data cache  
11 connected to said data transfer bus for temporarily storing data  
12 employed by said data processor, said data processor generating a  
13 data transfer request to said request queue controller for data  
14 writeback from said data cache to said system memory upon eviction  
15 of dirty data from said data cache.

1 24. (Original) The data processing system of claim 13,  
2 wherein:

3 said plurality of data processors, said request queue  
4 controller, said data transfer hub and said plurality of ports are  
5 disposed on a single integrated circuit.

1 25. (Currently Amended) The data processing system of claim  
2 13, further comprising:

3 a data memory having a data transfer bandwidth on the same  
4 order as a data transfer bandwidth of said data transfer hub;

5 ~~a second~~ an internal memory port connected to said data  
6 transfer hub and said data memory; and

7 said data transfer hub further controlling said source port  
8 and said destination port to not query said ~~second~~ internal memory  
9 port to determine if said destination port is capable of receiving  
10 data of a predetermined size if said ~~second~~ internal memory port is  
11 a destination port of a data transfer request.

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